ABSTRACT OF THE DISCLOSURE

A dynamic random access memory (DRAM) having pairs of bitlines, each pair being connected to a first bit line sense amplifier, wordlines crossing the bitlines pairs forming an array, charge storage cells connected to the bitlines, each having an enable input connected to a wordline, the bit line sense amplifiers being connected in a two dimensional array, pairs of primary databuses being connected through first access transistors to plural corresponding bit line sense amplifiers in each row of the array, apparatus for enabling columns of the first access transistors, databus sense amplifiers each connected to a corresponding data bus pair, a secondary databus, the secondary databus being connected through second access transistors to the databus sense amplifiers, and apparatus for enabling the second access transistors, whereby each the primary databus pair may be shared by plural sense amplifiers in a corresponding row of the array and the secondary databus may be shared by plural primary databus pairs.